## Laboratory Report Cover Sheet

**18ECE206J ADVANCED DIGITAL SYSTEMS DESIGN**

**Fourth Semester, 2021-22 (Even semester)**

SRM Institute of Science and Technology College of Engineering and Technology

Department of Electronics and Communication Engineering

#### Name :

**Register No. :**

**Day/ Session :**

**Venue :**

**Title of Experiment :**

**Date of Conduction :**

**Date of Submission :**

|  |  |  |
| --- | --- | --- |
| **Particulars** | **Max. Marks** | **Marks**  **Obtained** |
| Pre lab and Post lab | 10 |  |
| Lab Performance | 20 |  |
| Simulation and results | 10 |  |
| Total | 40 |  |

**REPORT VERIFICATION**

**Staff Name : Signature :**

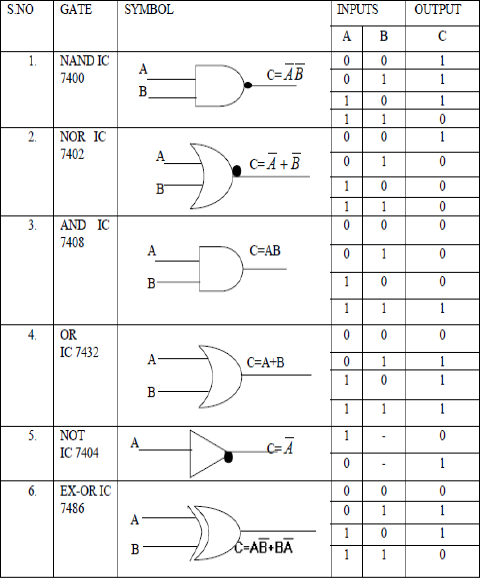
**5. Implementation of basic logic gates using VHDL**

**Aim:**

To design basic logic gates using VHDL.

**Software requirement:**

Xilinx-ise & Modelsim

**Theory:** A logic gate is a building block of a [digital](https://whatis.techtarget.com/definition/digital) [circuit.](https://whatis.techtarget.com/definition/circuit) Most logic gates have two inputs and one output and are based on [Boolean](https://whatis.techtarget.com/definition/Boolean) algebra. At any given moment, every terminal is in one of the two [binary](https://whatis.techtarget.com/definition/binary) conditions *false* (high) or *true* (low). False represents 0, and true represents 1. Depending on the type of logic gate being used and the combination of inputs, the binary output will differ. A logic gate can be thought of like a light switch, wherein one position the output is off—0, and in another, it is on—1. Logic gates are commonly used in integrated circuits ([IC](https://whatis.techtarget.com/definition/integrated-circuit-IC)).

#### VHDL CODE

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL; use IEEE.STD\_LOG IC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

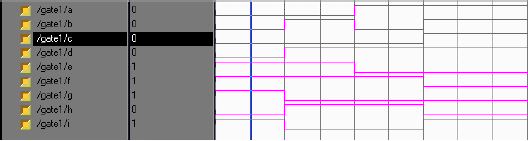
entity gates is

Port ( a,b : in std\_logic; c,d,e,f,g,h,i : out std\_logic); end gates;

architecture dataflw of gates is begin

c<= a and b; d<= a or b; e<= not a; f<= a nand b; g<= a nor b; h<= a xor b; i<= a xnor b; end dataflw;

#### Modelsim Output:



**Pre-lab Questions:**

1. Define Entity and architecture with format and example.
2. How many architectures are present in VHDL?
3. Why NAND and NOR are called as universal gates?

**Post-lab Questions:**

1. What is a test bench in VHDL?
2. Implement the following Boolean expression using logic gates in VHDL
   1. F=AC+A’BC’+ABC’
3. Realize a half Subtractor using universal gates.
4. Implement Full adder using only nand gate.

**Result:**